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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/809,809

03/26/2004

Tetsuya Ikuta

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08/09/2006

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EXAMINER

LE, THAO X

ART UNIT

PAPER NUMBER

2814

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/809,809	Applicant(s) IKUTA ET AL.	
	Examiner Thao X. Le	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 June 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) 1-9 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 9-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 9-12 and 14-19 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over US 6133605 to Kishi.

Regarding claim 9, Kishi discloses a manufacturing method of a semiconductor device in fig. 6-20 comprising the steps of: forming a gate insulation film 31, fig. 20, over a silicon substrate 1, col. 6 line 43(inherently semiconductor comprises silicon); and forming a gate electrode 9, fig. 12, over said gate insulation film 31, said step of forming a gate insulation film 31 including the steps of: forming a silicon oxide film 24, column 12 line 6, over said silicon substrate 1, said silicon oxide film 24 having a thickness of 1.5 nm or less, col. 12 line 9, and introducing nitrogen, column 12 line 16, into said silicon oxide film 24 and displacing silicon atoms on a surface of said silicon substrate toward said gate insulation film side, fig. 19.

The recitation of 'displacing silicon atoms on a surface of said silicon substrate toward said gate insulation film side', Kishi discloses a products that are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ

430, 433 (CCPA 1977) and MPEP 2112.01. See also 2004/0248392 (Narwankar) for the effects of thermal nitriding in [0040].

Regarding claim 10, Kishi discloses the method wherein said step of introducing nitrogen and displacing silicon atoms comprises the step of conducting a first heat treatment, column 9 line 5, to said silicon oxide film 24 in an ammonia atmosphere or nitrogen monoxide atmosphere, column 12 line 15-16.

Regarding claim 11, Kishi discloses the method wherein said gate insulation film 31 is formed over a region where a conductive type of said surface of said silicon substrate 1 is P-type, column 6 line 44.

Regarding claim 12, Kishi discloses a manufacturing method of a semiconductor device in fig. 6-15 comprising the steps of: forming a gate insulation film 31, fig. 20, over a silicon substrate 1; and forming a gate electrode 9 over said gate insulation film 31, said step of forming a gate insulation film including the steps of: forming a silicon oxide film 24 over said silicon substrate 1; said silicon oxide film having a thickness of 1.5 nm or less, col. 12 line 9; and introducing nitrogen, column 12 line 16, into said silicon oxide film 24, displacing silicon atoms on a surface of said silicon substrate 1 in a region where a conductive type of said surface is P-type, column 6 line 44, below said gate insulation film 31 toward said gate insulation film side, and displacing silicon atoms on said surface in a region where said conductive type of said surface is N-type 10, column 12 line 45, below said gate insulation film 31 toward an inner side of said silicon substrate 1.

The recitation of 'displacing silicon atoms on a surface of said silicon substrate toward said gate insulation film side', Kishi discloses a products that are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Regarding claim 13, Kishi discloses the method wherein said step of introducing nitrogen and displacing silicon atoms comprises the step of conducting a first heat treatment, column 12 line 16, to said silicon oxide film 24 in a ammonia atmosphere or nitrogen monoxide atmosphere, column 12 line 65, in said region where the conductive type of said surface is P-type, and conducting a plasma nitridation treatment, column 9 lines 4-8, to said silicon oxide film 24 in an ammonia atmosphere or nitrogen monoxide atmosphere, column 9 line 5, in said region where the conductive type of said surface is N-type 10.

Regarding claim 14, Kishi discloses the method according to claim 10, wherein said first heat treatment is conducted at 775 degree C or higher, col. 12 line 16.

Regarding claim 15, Kishi discloses the method wherein said step of forming a gate insulation film 31 comprises the step of forming a silicon nitride film 5, column 9 line 23, or high dielectric constant film over said silicon oxide film by deposition method, after said step of introducing nitrogen and displacing silicon atoms, fig. 11.

Regarding claim 16, Kishi discloses the method wherein said step of forming a gate insulation film 31 comprises the step of conducting a second heat treatment,

column 9 line 31, to said silicon oxide film, to which nitrogen has been introduced, after said step of forming a silicon nitride film or high dielectric constant film.

Regarding claim 17, Kishi discloses the method wherein said second heat treatment is conducted at a higher temperature than that at which said silicon nitride film or high dielectric constant film is formed, column 9 line 31.

Regarding claim 18, Kishi discloses the method wherein said step of forming a gate insulation film 31 comprises the steps of, after said step of introducing nitrogen and displacing silicon atoms: forming a high dielectric constant film over said silicon oxide film 24; conducting a second heat treatment to said silicon oxide film, column 9 line 8, to which nitrogen has been introduced; and forming a silicon nitride film 4, column 9 line 10 over said high dielectric constant film.

Regarding claim 19, Kishi discloses the method wherein said second heat treatment is conducted in a nitrogen monoxide atmosphere, column 9 line 9.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 6133605 to Kishi in view of JP 200332009 to Kataoka or US 2005/0130448 to Olsen et al.

Regarding claim 13, Kishi discloses the method wherein said step of introducing nitrogen and displacing silicon atoms comprises the step of conducting a first heat treatment, column 12 line 16, to said silicon oxide film 24 in a ammonia atmosphere or nitrogen monoxide atmosphere, column 12 line 65, in said region where the conductive type of said surface is P-type,

But, Kishi does not disclose conducting a plasma nitridation treatment to silicon oxide film in an ammonia atmosphere or nitrogen monoxide atmosphere in region where the conductive type of said surface is N-type 10 (PMOS region).

However, Kataoka discloses a PMOS transistor wherein the gate oxide is being plasma nitriding [0005]. In addition, Olsen discloses plasma nitriding the silicon oxide layer for the PMOS transistor [0009]. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the plasma nitriding the PMOS gate oxide teaching of Kataoka with Kishi, because it would have controlled the fluctuation of the threshold voltage of the PMOS

transistor as taught by Kataoka [0005] or because it would have formed a high PMOS drive current and a low gate leakage as taught by Olsen [0009].

Response to Arguments

6. Applicant's arguments with respect to claims 9-19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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A handwritten signature in black ink, consisting of several overlapping horizontal and diagonal strokes, positioned above the printed name.

Thao X. Le
31 July 2006